STA2000

PDA-PLATFORM SYSTEM-ON-CHIP

PRODUCT PREVIEW

FEATURES

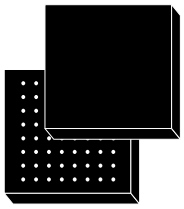
- ARM9TDMI CPU, with 16Kbytes of I&D cache, MMU supporting 32 and 16 bit instruction sets
- Configurable PLL for selectable processor speed
- 40Kbytes on-chip embedded SRAM used to store the video frame buffer. The colour LCD controller supports ¼ VGA to VGA at 1,2,4,8 and 16 Bits per Pixel, at 80Hz refresh. There is a separate DMA interface to the LCD controller
- Memory controller for SDRAM, SRAM and the PCMCIA interface. The expansion and ROM interface gives 8 x 256 Mbyte expansion segments with independent wait state control. Selectable boot sources from either ROM or Synchronous ROM or Synchronous FLASH orregular FLASH.
- Interrupt and fast interrupt controller
- 60 bits of GPIO for keyboard control
- 10 channel DMA support for LCD, USB, AC97 and MMC allowing streaming mode operation
- IrDA SIR protocol capable of speeds up to 115Kbps, as part of UART1
- Three 16 bit general purpose counter timers
- A 32 bit real time clock and comparator
- Support for Multi-ICE

STATISTICS

- 0.18µ CMOS process
- Core supply voltage 1.8 with 3.3V I/Os
- 256 pin fine pitch BGA package
- ARM920T core operates up to 200MHz at 1.8V.
- AHB Bus operates up to 100MHzMHz at 1.8V (temperature in consumer range only).
- External memory interface operates up to 100MHz at 1.8V

APPLICATIONS

- STA 2000 facilitates applications in mobile Internet and personal multimedia devices. Services include voice, messaging, PIM, office and Internet.
- Smartphones
- PDA
- Communicators
- WID -Wireless Internet devices
- Screenphones/Internet appliances
- Point of Sales Terminals



PACKAGE BGA256
ORDERING NUMBER: STA2000

DESCRIPTION

The STA2000 is the system-on-chip device designed for PDAs, advanced cellular phones and other wireless internet devices.

The SoC uses the ARM920T processor with the AMBA bus architecture. It has a typical operating spec of 200MHz at 1.8V. The SoC also includes 40Kbytes of embedded memory for storing LCD images.

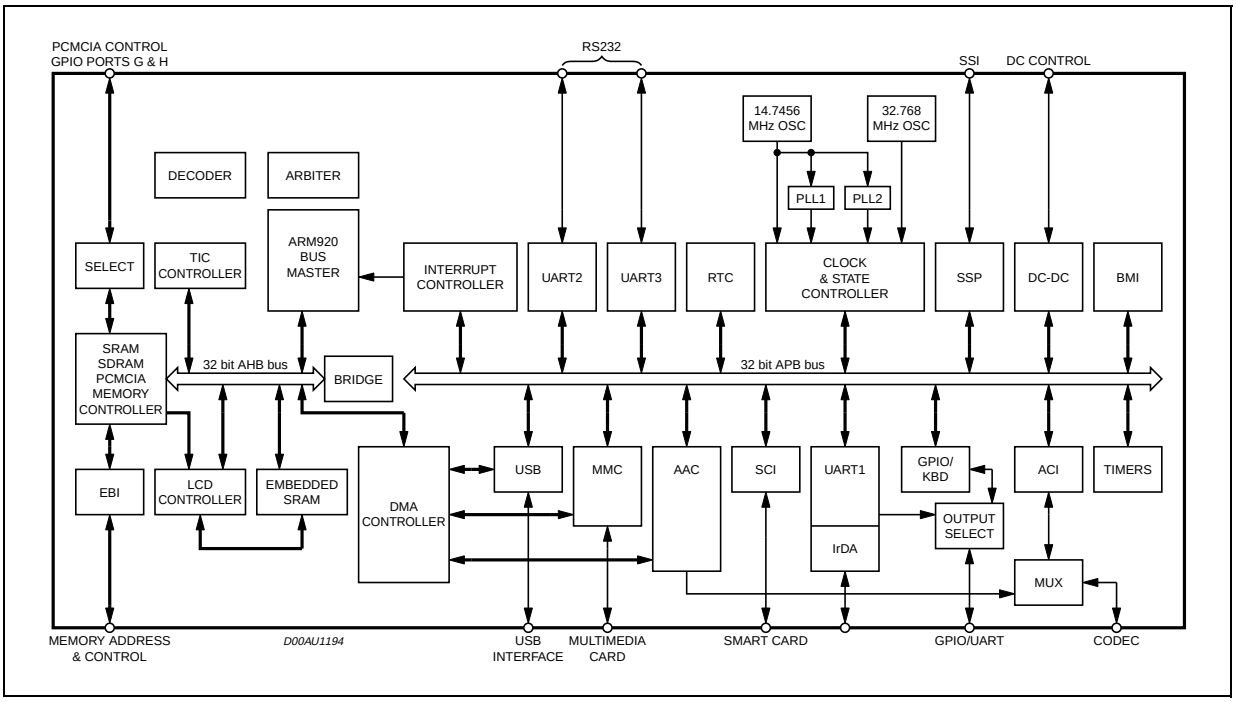
The STA2000 has been specifically designed with power management as a priority. The low power design was achieved using sub peripheral gating that disables blocks when not in use. The use of three modes of operation also facilitates power optimisation.

The SoC can operate in various processor and memory configurations, allowing the power/performance profile to be tailored to the customer.

The following Interfaces are provided:

- Multimedia Card Interface with 20Mbps bandwidth
- USB Function (or Slave) Interface with 12Mbps bandwidth
- 3 Full duplex UART's, each with two 16 byte FIFO memories up to 460kbps bandwith
- Synchronous serial port for Microwire or SPI peripherals such as ADC's
- Advanced Audio Codec Interface
- Audio Codec Interface
- Two DC to DC converter interfaces
- Smart Card Interface and Battery MonitorInterface

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	2.5	V
V_{IN}	DC Input Voltage	4	V
V_{OUT}	DC Output Voltage	4	V
I_{LATCH}	Latch Up Current	±100	mA
T_{stg}	Storage and Junction Temperature	-65 to 150	°C

ELECTRICAL CHARACTERISTCS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	DC Supply Voltage	3.3 I/O	3.0	3.3	3.6	V
	Core DC Supply Voltage	1.8 Core	-5%	1.8	+5%	V
T_B	Operating Temperature Range		-40		85	°C

FUNCTIONAL DESCRIPTION

Internal Architecture

The STA2000 is based on the ARM920T RISC processor. The ARM920T is a member of the ARM9 family of general purpose microprocessors. The ARM920T supports two alternative instruction sets, the 32-bit ARM operating mode and 16-bit Thumb mode allowing the user to trade off between high performance and high code density. The ARM920T supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM920T also includes support for coprocessors. The ARM920T is a Harvard cache architecture processor. The separate instruction and data caches in this design are 16KB each in size, with an 8-word line length. The ARM920T implements an enhanced ARM Architecture V4 MMU (Memory Management unit) to provide translation and access permission checks for instruction and data addresses. The ARM920T interface to the rest of the system is via unified address and data buses. For co-processor support the instruction and data buses are exported along with simple handshaking signals.

The processor operates up to 200MHz in the 0.18µ CMOS process technology.

ARM Core

The processor core within ARM920T is an ARM9TDMI. This processor core is a Harvard architecture device implemented using a five-stage pipeline consisting of fetch, decode, execute, memory and write stages.

Power Management Features

The STA2000 has three basic power states.

- The halt mode stops the ARM920T while HCLK stays running, allowing DMA transfers to complete.
- In the standby mode all the clocks are stopped apart from 32 KHz and derivatives. This is basically a shutdown state. The clocks recover on wakeup or interrupt. All system memory and states are maintained. The SRAM's are put into self refresh mode.
- In the run mode the device runs normally. Power saving is also achieved by disabling blocks when not in use. Software controlled clock gating masks the peripheral primary clock and its version of PCLK. Each peripheral has an enable bit that when set will enable its primary clock and its own version of PCLK. This saves power in both idle and running states by allowing the minimum system to be clocked.

Configurable PLL

The use of two PLLs in STA2000 enables processor speeds up to 200MHz to be selected. One PLL (PLL2) is used to generate a fixed frequency of 48MHz, this is used to drive the USB Slave peripheral. The other PLL (PLL1) provides a programmable frequency up to the maximum limit and is used to create the main clock for the ARM920T. The 14MHz clock is used to provide the frequency input to both the PLLs.

Memory Control

The ARM920T and the DMA engine share the main system bus providing access to all external memory devices

and the buffer. The LCD controller has access to embedded SRAM frame buffer and an extension buffer in SDRAM for dual panel or large displays.

Static Memory Controller

The static memory controller provides access to static memory devices on the external bus, and can be used to interface to a wide variety of external device types, including SRAM, ROM, PC-Cards and CF-Cards. Eight memory spaces are provided, each with a set of registers that determines the timing characteristics made to that space. Six are general purpose and the remaining two provide an interface to PC and CF Card devices. The controller also supports static memory devices in burst or page mode.

SDRAM Controller

The SDRAM controller controls the external SDRAM. Up to four Synchronous Memory banks can be independently set up with features including

- Special configuration bits for Synchronous ROM operation.
- An ability to programme Synchronous Flash devices using write and erase commands.
- On booting from Synchronous ROM, (and optionally with Synchronous Flash), a configuration sequence is performed before releasing the processor form reset.
- Data is transferred between the controller and the SDRAM in quad word bursts. Longer transfers will be concatenated forming a seamless burst.
- Programmable for 16 or 32 bit data busses.
- Power saving Synchronous Memory CKE and external clock modes provided.
- Two reset domains are provided to enable SDRAM contents to be preserved over a soft reset.

Smart Card Interface

The SCI can autonomously control data transfer to and from the smart card. Transmit and receive FIFOS are provided to reduce the required interaction between the CPU and the peripheral. The following features are also provided by the SCI.

- Support for synchronous smart cards.
- Asynchronous T0 and T1 transmission protocols.
- Direct interrupts for TX and RX FIFO level monitoring.
- Hardware initiated card deactivation sequence on detection of a card removal.
- Software initiated card deactivation sequence on transaction complete.

Battery Monitor Interface

The BMI (Battery Monitor Interface) used in the STA2000 is a Smart Battery interface that uses a two-wire multi-master bus, meaning that more than one device capable of controlling the bus can be connected to it. Since more than one device may attempt to take control of the bus as a master the smart battery interface provides an arbitration mechanism based on I2C. In addition to bus arbitration the Smart Battery implements the I2C method of clock extending in order to accommodate devices of different speeds on the same bus.

Advanced AUDIO CODEC

The AAC LINK is a 5-pin serial interface to the audio codec. It is a bi-directional fixed rate, serial PCM (Pulse Code Modulation) digital stream, dividing each audio frame into 12 out-going and 12 incoming data streams, each with 20-bit sample resolution. The AAC controller performs the following functions

- Serial-to-parallel conversion on data received from the peripheral device

– Parallel-to-serial conversion on data transmitted to the peripheral device

The CPU reads and writes control and status information via the AMBA APB interface. The transmit and receive paths are buffered with internal FIFO memories allowing data to be stored independently in both transmit and receive modes.

The controller has four channels that consist of a transmit FIFO, receive FIFO and their associated control logic.

Interrupt Control

All interrupts in STA2000 are directed through the interrupt controller. The interrupts are derived from two sources; external interrupts input directly from the pins and interrupts originating from the peripherals. The interrupt controller controls the interrupts from 28 different sources. Four interrupt sources are mapped to the FIQ input of the ARM920T and 24 are mapped to the IRQ input. After a power on reset all mask register bits are cleared, this has the effect of masking all the interrupts. As a result, enabling of the mask register must be done by software after a power-on-reset.

USB

The USB hardware consists of a Serial Interface Engine and a Serial Interface Unit. The USB provides a high level interface that shields the firmware from the USB protocol details. The USB supports full speed (12 Mbps) functions and Suspend and Resume signalling. The block contains 4 endpoints each terminated with dedicated FIFOs. The byte depth of the FIFO is 16 bytes. These endpoints are used for control transfers, bulk input transfers, bulk output transfers and interrupt in transfers. The USB is fully compatible with both Open HCI and Intel UHCI standards.

UART Interface

The STA2000 contains three UARTs with the following functionality.

– Baud rate generator containing free running counter, which generate internal ÷16 clocks.

– An 8-bit wide and 16-word depth transmit FIFO memory buffer.

– An 11-bit wide and 16-word depth receive FIFO memory buffer.

– Transmit logic that performs parallel-to-serial conversion on the data read from the transmit FIFO.

Free Running Counters

There are three counters integrated into the STA2000; two of them are identical. Each of these counters has a 16-bit read/write register and a control register. Each counter is loaded with a value written to the data register. This value will be decremented and when the timer counter reaches 0, it will assert the appropriate interrupt. The first two counters can run at 508KHz or 2KHz depending on the value written into the control register. The third counter has the same basic operation but it is clocked at 7.3728MHz.

Real Time Clock

The real time clock peripheral can be used to provide a basic alarm function or a long timer base counter. This is achieved by generating an interrupt signal after counting down for a programmed number of cycles of a real time clock input. The main features are

– 32-bit counter with programmable load.

– Programmable 32-bit match compare register.

– Software maskable interrupt when counter and compare registers are identical.

Bus Arbitration

The following are the four main areas of the bus arbitration.

The Main AHB system bus arbiter.

This arbiter controls the bus master arbitration for the AHB bus. The AHB bus has three Master interfaces; these are the ARM920T, the DMA controller and the TIC controller. These interfaces have an order of priority closely linked with the power saving modes. The power saving modes of halt and standby force the arbiter to grant the default bus master. As the default bus driver is the TIC controller and is not activated during normal mode the TIC will drive default values on the system bus and will remain idle.

The Embedded SRAM slave interface arbiter and the SDRAM slave interface arbiter

Both the SDRAM controller and the Embedded SRAM have slave interfaces to the main AHB and the LCD controller DMA bus. In order to control the accesses to these memory systems each peripheral has an arbiter that prioritises between the AHB and LCD DMA bus. In both cases the LCD controller bus is given priority.

The EBI bus arbiter.

This arbiter is used to arbitrate between accesses from the Static Memory controller and the SDRAM controller. The priority will be given to accesses from the SDRAM controller.

EBI Block

The EBI block is required to interface to external memory. There can be up to 12 external memories made up of ROMs, SRAMs, SDRAMs, PCMCIA and CF cards. These external memories can be used for Boot Code and also for scratch RAM for the processor.

PDA platform 2000 has the option to boot from three different sources, ROM, SDROM or Synchronous Flash or Static Flash.

DC-DC Converter Interface

The DC-DC Converter interface is a dual-output Pulse Width Modulation (PWM) controller. It can be configured under software control by writing data via the AMBA APB interface to configure frequency and duty cycle of each output. The key features are

- Dual PWM drive outputs, with independent closed loop feedback.
- Software programmable configuration of one of four output frequencies.
- Software programmable configuration of duty cycle from 0 to 15/16, in intervals of 1/16.
- Each PWM drive output can be dynamically switched to one of a pair of pre-programmed frequency/ duty cycle combinations via external pins.

General Purpose I/O Peripheral

The GPIO provides 60 inputs/outputs organised as seven 8-bit groups and one 4-bit group, port A to Port H. Each port has an associated Data direction register and Data register.

Clock and State Controller

The primary function of the Clock and state controller is to control the gating and generation of the clocks in the PDA platform 2000. The clock domains used in PDAplatform 2000 are derived from two main sources, the 14.7456 MHz oscillator and the 32.768KHz real time clock oscillator. The 14.7456 MHz oscillator generates the supply to PLL1 that generates the bus and processor clocks, and the supply to PLL2 that generates 48MHz for the primary input clock to the USB peripheral. The 32.768KHz clock is used to drive a ripple divide chain that provides clocks for the RTC and the state controller. The Clock and state controller implements the clock gating and frequency dividers for all clock trees produced from these two oscillators. As the 32KHz clock tree produces the only permanently running clocks in the PDA platform 2000, these clocks are used to condition the wakeup signals and control the transition of the power saving states. The clocks generated by the 32KHz clocks are also

used to control interlocks that allow time for the PLL's to lock before a clock is supplied to the device.

DMA Controller

The DMA controller is used to interface streams from the USB, MMC and AAC peripherals to the system memory. The MMC and USB peripherals each use two DMA channels, one for transmit and one for receive. The AAC peripheral uses six DMA channels (three transmit and three receive) to allow different data sample frequency queues to be handled with low software overheads.

LCD Controller

The Colour LCD Controller's (CLCD) basic function is to send out the image data from system memory to an LCD panel by properly formatting the raw image data stored in memory. The colour LCD controller provides all the necessary control signals to interface directly to variety of colour and monochrome LCD module types. The block takes data from the SDRAM controller, providing data to the two FIFOs at the front end of the LCD controller data path, at a rate sufficient to support the chosen display mode and resolution.

The principal features of the LCD controller are

- Dual 32 stage by 32 bit FIFOs for buffering incoming display data.
- Supports single and dual panel colour and monochrome STN displays.
- Resolution programmable up to 1024 x 768 (bandwidth permitting).
- Single and dual panel mono STN displays with 4 or 8 bit interfaces.
- Supports TFT colour displays.
- 15 grey level mono 3375 colour STN, and 32K colour TFT support.
- 1,2 or 4bpp palletised displays for mono STN.
- 1,2,4 or 8bpp palletised colour displays for colour STN and TFT.
- "True-colour" non-palletised, for colour STN and TFT.
- 256 entry, 16 bit palette RAM, arranged as a 128 x 32 bit RAM physically.
- Programmable byte order and programmable pixel order within a byte.
- Patented greyscale algorithm.
- The LCD also incorporates a Memory Management Unit that will be able to contiguously map its on-chip and off chip memory areas. Typically the first 40Kbytes of data will be stored in the Embedded Static Memory, with the remainder being located within the external SDRAM memory.

Multi Media Card

The Multi Media Card (MMC) adapter is the link between the APB bus and the MultiMedia Card bus. It translates the protocol of the serial MultiMedia Card bus to the parallel APB bus and vice versa. The MMC adapter bus combines all of the requirements and functions of an MMC host.

The MMC controller uses the three-wire serial data bus (clock, command and data) to input and output digital data to and from the MMC card and to configure and acquire status information from the card registers.

Synchronous Serial Peripheral

The SSP (Synchronous Serial Peripheral) is a master-only interface with slave peripheral devices that has SPI, or Microwire synchronous serial interfaces.

The SSP performs serial-to-parallel conversion on data received from a peripheral device. The CPU reads and writes data and control/status information via the AMBA APB interface. The transmit and receive paths are buffered with internal FIFO memories allowing up to eight 16-bit values to be stored independently in both transmit and receive modes.

Audio Codec Interface

The Audio CODEC Interface provides a digital serial interface to an off-chip 8-bit CODEC. It also provides the timing required to serialise or deserialise the data stream to or from the CODEC device. Data and control/status information are written and read by the CPU. The interface supports full duplex operation and the transmit and receive paths are buffered with internal FIFO memories allowing up to 16 bytes to be stored independently in both transmit and receive modes with DMA support for 6 Rx and Tx Channels.